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10/650,451

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Subhas C. Bose Jayappa Veeramma

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TOWNSEND AND TOWNSEND AND CREW, LLP  
TWO EMBARCADERO CENTER  
EIGHTH FLOOR  
SAN FRANCISCO, CA 94111-3834

EXAMINER

NADAV, ORI

ART UNIT

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/650,451	<b>Applicant(s)</b> BOSE JAYAPPA VEERAMMA ET AL.	
	<b>Examiner</b> Ori Nadav	<b>Art Unit</b> 2811	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 September 2010.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3, 26, 28 and 30 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 26, 28 and 30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Objections***

Claim 1 is objected to because of the following informalities: The phrase “the first and second electrode terminals”, should read the first electrode terminal and the second electrode terminal”.

The phrase “the first and second conductive regions”, should read the first conductive region and the second conductive region”.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 30 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the specification for the claimed limitation of a power device being a diode, as recited in claim 30.

Art Unit: 2811

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-3, 26, 28 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitation of a power device being a diode, as recited in claim 30, is unclear as to whether the claimed device is a power device or a diode.

The claimed limitation of “the passivation layer includes an oxide layer”, as recited in claim 26, is unclear as to whether said oxide layer is the same element recited in claim 1, or the passivation layer comprises two oxide layers.

The claimed limitation of “the passivation layer comprising a polyimide layer over and oxide layer”, as recited in claim 1, is unclear as to the structural relationship between the passivation layer the oxide layer and the polyimide layer.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2811

Claims 1-3, 26, 28 and 30, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano (5,138,415) in view of Gross (5,316,964), Patterson (4,972,247), Vyne (4,606,781) and Moss et al. (5,024,922).

Yano teaches in figure 2 and related text a power device, comprising:

- a semiconductor substrate 16 of first conductivity having an upper surface and a lower surface;

- a first electrode terminal 29 coupled to a first conductive region 24 provided proximate the upper surface of the substrate, the first electrode terminal being provided over the upper surface of the substrate;

- a second electrode terminal 36 coupled to a second conductive region 18 provided proximate the lower surface of the substrate, the second electrode terminal being provided below the lower surface of the substrate;

- an isolation diffusion region 17 of second conductivity P provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface; and

- a passivation layer 28 provided over the upper surface of the substrate, the first surface of the isolation diffusion region;

wherein the first and second electrode terminals define a vertical electrical current path there between, and

wherein the peripheral junction region is provided to compensate the surface depletion of the isolation diffusion region.

Yano does not teach a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, wherein the peripheral junction region is different than the first and second conductive regions, and wherein the passivation layer comprising a polymid layer over and oxide layer.

Gross teaches in figure 2 and related text a peripheral junction region of second conductivity N<sup>+</sup> formed at least partly within an N type isolation diffusion region 16, 17 and formed proximate the first surface of the isolation diffusion region.

Patterson teaches in figure 2 and related text a peripheral junction region of second conductivity 19 formed at least partly within an isolation diffusion region 12 and formed proximate the first surface of the isolation diffusion region.

Vyne teaches in figure 4 and related text a passivation layer 44 comprising a polymid layer over and oxide layer.

Moss et al. teach in figure 4 and related text the advantages of using a passivation layer comprising a polymid layer over and oxide layer (see column 8, lines 18-22).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a peripheral junction region of second conductivity at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, wherein the passivation layer comprising a polymid layer over and oxide layer, in Yano's device in order to provide better

Art Unit: 2811

protection to the device and to increase the electrical isolation capabilities of the device.

The combination is motivated by the teachings of Gross who points out the advantages of using a peripheral junction region within the isolation junction region (column 2, lines 38-41), and by the teachings of Moss et al. who point out the advantages of using a passivation layer comprising a polyimide layer over an oxide layer (see column 8, lines 18-22).

Note that prior art's device includes a peripheral junction region being different than the first and second conductive regions.

Regarding claim 26, prior art's device includes a passivation layer includes an oxide layer and contacts the upper surface of the substrate, the first surface of the isolation diffusion region, and the peripheral junction region.

Regarding claim 28, the claimed limitations of "the peripheral junction region is provided to compensate the surface depletion of dopants in the isolation diffusion region and increase a reverse blocking voltage of the device by reducing an electric field at the first surface of the isolation diffusion region" are inherent in prior art's device, because prior art's device comprises a peripheral junction region which compensates the surface depletion of dopants in the isolation diffusion region and increase a reverse blocking voltage of the device by reducing an electric field at the first surface of the isolation diffusion region, as claimed.

Art Unit: 2811

Regarding claim 30, Yano teaches a first electrode terminal being separated from the isolation diffusion region. Regarding the claimed limitation of “the device is a diode”, it is noted that independent claim 1 recites a power device. Clearly, a diode is not a power device. Therefore, it is understood that the diode is part of the power device. Thus, Yano’s structure comprises a diode (e.g. layers 16 and 18 form a diode).

Claims 1-3, 26, 28 and 30, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Gross (5,316,964), Patterson (4,972,247), Vyne (4,606,781) and Moss et al. (5,024,922).

AAPA teaches in figure 1 and related text a power device, comprising:

- a semiconductor substrate 1 of first conductivity having an upper surface and a lower surface;

- a first electrode terminal 7 coupled to a first conductive region 5 provided proximate the upper surface of the substrate, the first electrode terminal being provided over the upper surface of the substrate;

- a second electrode terminal 16 coupled to a second conductive region 15 provided proximate the lower surface of the substrate, the second electrode terminal being provided below the lower surface of the substrate;



an isolation diffusion region 2 of second conductivity P provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface; and

a passivation layer 17 provided over the upper surface of the substrate, the first surface of the isolation diffusion region;

wherein the first and second electrode terminals define a vertical electrical current path there between, and

wherein the peripheral junction region is provided to compensate the surface depletion of the isolation diffusion region.

AAPA does not teach a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, wherein the peripheral junction region is different than the first and second conductive regions, and wherein the passivation layer comprising a polyimide layer over an oxide layer.

Gross teaches in figure 2 and related text a peripheral junction region of second conductivity N<sup>+</sup> formed at least partly within an N type isolation diffusion region 16, 17 and formed proximate the first surface of the isolation diffusion region.

Patterson teaches in figure 2 and related text a peripheral junction region of second conductivity 19 formed at least partly within an isolation diffusion region 12 and formed proximate the first surface of the isolation diffusion region.

Art Unit: 2811

Vyne teaches in figure 4 and related text a passivation layer 44 comprising a polyimide layer over and oxide layer.

Moss et al. teach in figure 4 and related text the advantages of using a passivation layer comprising a polyimide layer over and oxide layer (see column 8, lines 18-22).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a peripheral junction region of second conductivity at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, wherein the passivation layer comprising a polyimide layer over and oxide layer, in AAPA's device in order to provide better protection to the device and to increase the electrical isolation capabilities of the device.

The combination is motivated by the teachings of Gross who points out the advantages of using a peripheral junction region within the isolation junction region (column 2, lines 38-41), and by the teachings of Moss et al. who point out the advantages of using a passivation layer comprising a polyimide layer over and oxide layer (see column 8, lines 18-22).

Note that prior art's device includes a peripheral junction region being different than the first and second conductive regions.

Regarding claim 26, prior art's device includes a passivation layer includes an oxide layer and contacts the upper surface of the substrate, the first surface of the isolation diffusion region, and the peripheral junction region.

Regarding claim 28, the claimed limitations of “the peripheral junction region is provided to compensate the surface depletion of dopants in the isolation diffusion region and increase a reverse blocking voltage of the device by reducing an electric field at the first surface of the isolation diffusion region” are inherent in prior art’s device, because prior art’s device comprises a peripheral junction region which compensates the surface depletion of dopants in the isolation diffusion region and increase a reverse blocking voltage of the device by reducing an electric field at the first surface of the isolation diffusion region, as claimed.

Regarding claim 30, AAPA teaches a first electrode terminal being separated from the isolation diffusion region. Regarding the claimed limitation of “the device is a diode”, it is noted that independent claim 1 recites a power device. Clearly, a diode is not a power device. Therefore, it is understood that the diode is part of the power device. Thus, AAPA’s structure comprises a diode (e.g. layers 15 and 1 form a diode).

Claims 1 and 30, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama (5,994,189) in view of Gross, Patterson, Vyne and Moss et al.

Art Unit: 2811

Regarding claim 1, Akiyama teaches in figure 1 and related text a power device, comprising:

- a semiconductor substrate 2 of first conductivity having an upper surface and a lower surface;

- a first electrode terminal 11 coupled to a first conductive region 4 provided proximate the upper surface of the substrate, the first electrode terminal being provided over the upper surface of the substrate;

- a second electrode terminal 13 coupled to a second conductive region 1 provided proximate the lower surface of the substrate, the second electrode terminal being provided below the lower surface of the substrate;

- an isolation diffusion region 7 of second conductivity P provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface; and

- a passivation layer 10 provided over the upper surface of the substrate, the first surface of the isolation diffusion region;

wherein the first and second electrode terminals define a vertical electrical current path there between, and

wherein the peripheral junction region is provided to compensate the surface depletion of the isolation diffusion region.

Akiyama does not teach a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate

Art Unit: 2811

the first surface of the isolation diffusion region, wherein the peripheral junction region is different than the first and second conductive regions, and wherein the passivation layer comprising a polymid layer over and oxide layer.

Gross teaches in figure 2 and related text a peripheral junction region of second conductivity N+ formed at least partly within an N type isolation diffusion region 16, 17 and formed proximate the first surface of the isolation diffusion region.

Patterson teaches in figure 2 and related text a peripheral junction region of second conductivity 19 formed at least partly within an isolation diffusion region 12 and formed proximate the first surface of the isolation diffusion region.

Vyne teaches in figure 4 and related text a passivation layer 44 comprising a polymid layer over and oxide layer.

Moss et al. teach in figure 4 and related text the advantages of using a passivation layer comprising a polymid layer over and oxide layer (see column 8, lines 18-22).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a peripheral junction region of second conductivity at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, wherein the passivation layer comprising a polymid layer over and oxide layer, in Akiyama's device in order to provide better protection to the device and to increase the electrical isolation capabilities of the device.

The combination is motivated by the teachings of Gross who points out the advantages of using a peripheral junction region within the isolation junction

Art Unit: 2811

region (column 2, lines 38-41), and by the teachings of Moss et al. who point out the advantages of using a passivation layer comprising a polyimide layer over an oxide layer (see column 8, lines 18-22).

Note that prior art's device includes a peripheral junction region being different than the first and second conductive regions.

Regarding claim 30, Akiyama teaches in figure 1 and related text a device being a diode 1, 2, 4, wherein the first electrode terminal being separated from the isolation diffusion region.

Claims 1 and 30, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori et al. (5,101,244) in view of Gross, Patterson, Vyne and Moss et al.

Regarding claim 1, Mori et al. teach in figure 1A and related text a power device, comprising:

- a semiconductor substrate 14 of first conductivity having an upper surface and a lower surface;

- a first electrode terminal 3 coupled to a first conductive region 16 provided proximate the upper surface of the substrate, the first electrode terminal being provided over the upper surface of the substrate;

- a second electrode terminal 2 coupled to a second conductive region 13 provided proximate the lower surface of the substrate, the second electrode terminal being provided below the lower surface of the substrate;

a passivation layer 4 provided over the upper surface of the substrate, the first surface of the isolation diffusion region;

wherein the first and second electrode terminals define a vertical electrical current path there between, and

wherein the peripheral junction region is provided to compensate the surface depletion of the isolation diffusion region.

Mori et al. do not teach an isolation diffusion region of second conductivity provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface; and a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, wherein the peripheral junction region is different than the first and second conductive regions, and wherein the passivation layer comprising a polymid layer over and oxide layer.

Gross teaches in figure 2 and related text an isolation diffusion region 16, 17 of second conductivity provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface, and a peripheral junction region of second conductivity N<sup>+</sup> formed at least partly within an N type

Art Unit: 2811

isolation diffusion region 16, 17 and formed proximate the first surface of the isolation diffusion region.

Patterson teaches in figure 2 and related text an isolation diffusion region 12 of second conductivity provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface, and a peripheral junction region of second conductivity 19 formed at least partly within an isolation diffusion region 12 and formed proximate the first surface of the isolation diffusion region.

Vyne teaches in figure 4 and related text a passivation layer 44 comprising a polyimide layer over and oxide layer.

Moss et al. teach in figure 4 and related text the advantages of using a passivation layer comprising a polyimide layer over and oxide layer (see column 8, lines 18-22).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an isolation diffusion region of second conductivity provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface, and a peripheral junction region of second conductivity at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, and wherein the



Art Unit: 2811

passivation layer comprising a polymid layer over and oxide layer, in Mori et al.'s device in order to provide protection to the diode and in order to increase the electrical isolation capabilities of the device.

The combination is motivated by the teachings of Gross who points out the advantages of using a peripheral junction region within the isolation junction region (column 2, lines 38-41), and by the teachings of Moss et al. who point out the advantages of using a passivation layer comprising a polymid layer over and oxide layer (see column 8, lines 18-22).

Note that prior art's device includes a peripheral junction region being different than the first and second conductive regions.

Regarding claim 30, Mori et al. teach in figure 1A and related text a device being a diode, wherein the combined device includes the first electrode terminal being separated from the isolation diffusion region (see Patterson et al.).

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-3, 26, 28 and 30 have been considered but are moot in view of the new ground(s) of rejection.

Art Unit: 2811

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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/ORI NADAV/  
PRIMARY EXAMINER  
TECHNOLOGY CENTER 2800